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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,040	07/11/2003	Yutaka Ito	Q76480	3063

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,040	ITO ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *19 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/19/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicants' response was received May 19, 2006.

- Claims 1-7 and 9-15 stand rejected.
- Corrected drawings are accepted.
- Abstract is accepted.
- Title is accepted.
- Claim objections are withdrawn.
- Claim rejections under 35 USC 112 are withdrawn.

Application pending.

Response to Amendment

Applicants' arguments/amendments with respect to amended claims 1-3 and 9-11 and previously presented claims 4-7 and 12-15 filed May 19, 2006 have been received. All arguments have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

In response to Applicants' argument that the references fail to show certain features of Applicants' invention, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). For example, Applicants contend the prior art does not teach or suggest, "...independent data mask blocks controlled by independent data mask signals..." Although the

claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The Examiner disagrees with the Applicants and maintains rejections with respect to amended claims 1-3 and 9-11 and previously presented claims 4-7 and 12-15. All arguments have been considered. It is the Examiner's conclusion that amended claims 1-3 and 9-11 and previously presented claims 4-7 and 12-15, as presented, are not patentably distinct or non-obvious over the prior art of record.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-7 and 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemae (USPN 4688219) further in view of Fifield (USPN 5307356).

As per claim 1, Takemae substantially teaches to check for errors in a memory using parity checking techniques and to correct the detected errors using redundant memory cells. Takemae teaches a semiconductor memory device (col. 1, line 65) with a parity portion and a redundant portion (col. 1, lines 66-68). Takemae teaches an error correcting circuit (col. 2, lines

14-15) to perform error correction. Takemae also teaches to combine the redundant correcting and parity checking process as stated in the present application.

Takemae does not explicitly teach the error correction circuit to use a Hamming code for the correction process as stated in the present application.

However, Fifield, in an analogous art, substantially teaches (abstract) a DRAM which includes an on-chip ECC system. Particularly, Fifield teaches (col. 6, lines 4-23) the error correction circuit to use Hamming code. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a Hamming code for the correction process in the error correction circuit within the method and apparatus of Takemae. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by utilizing a Hamming code within the error correction circuitry would have improved the error detection and correction capability.

As per claim 2, Takemae substantially teaches, in view of above rejections, (col. 1, lines 17-22) when a defective memory cell is selected to be read, the redundant memory cell is actually read in place of the defective memory cell, so that the correct data can be read.

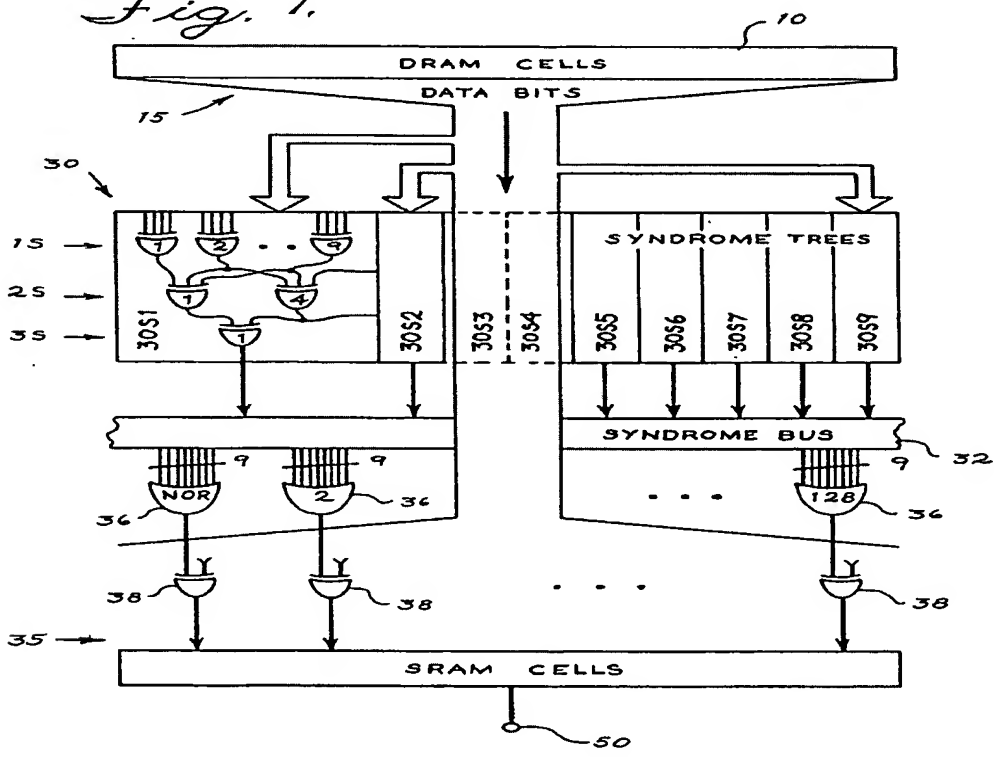
As per claim 3, Fifield substantially teaches, in view of above rejections, (col. 6, lines 2-23) a Hamming code used in the error correcting circuit which is able detect a double error or correct a single error. The Examiner would like to point out that Hamming codes are known to have such standardized properties and in fact all error-correcting codes are limited in correcting detected errors. Furthermore, if the code word is found to have more errors than that are correctable, usually it has to be replaced with a redundant code word.

As per claim 4, Takemae substantially teaches, in view of above rejections, (col. 2) the error correcting circuit includes a data selector, operatively connected to the memory cell array, for receiving read data from a plurality of memory cells including a selected memory cell. The data selection also selectively outputs a part of the read data which forms horizontal and vertical parity-checking groups corresponding to a parity-checking two-dimensional virtual matrix. A vertical parity generator and a horizontal parity generator are connected to the data selector, for generating a vertical parity and a horizontal parity of the data group, respectively. In addition, a parity storing memory for storing a previously determined vertical parity and a previously determined horizontal parity are included along with a comparator connected to the vertical and horizontal parity generators and to the parity storing memory. The comparator compares the outputs of the inhibit and parity generating circuit with the previously determined vertical and horizontal parities so as to correct an error in the read data.

As per claims 5-7, Fifield substantially teaches, in view of above rejections, (Figure 1) syndrome generator 30S1, each generator (or "syndrome tree") is made up of three stage exclusive-OR (XOR) logic trees. The first stage 1S of the logic tree is made up of a first set of four-input XOR gates; the second stage 2S is made up of approximately four four-input XOR gates; and the final stage 3S is a single four-input XOR gate. Note that the syndrome generators 30S1-30S9 have different numbers of inputs (specifically 51, 59, 59, 59, 55, 59, 60, 47, and 56 respectively) to optimize the interconnect wiring layout. The three stages of XOR of one syndrome generator provide the parity of a subset of the one hundred and twenty eight data bits. This generated parity bit is then compared to a corresponding one of the stored check bits for that error correction word. The comparison operation, which is the XOR of a specific subset of PDL

lines 15 and their corresponding stored check bits is executed by 1S, 2S and 3S. For the purposes of illustration, assume the arrowhead going into bus 32 is the result of this XOR operation. This XOR result is referred to as a syndrome bit, which is coupled to a respective line of a syndrome bus 32. The syndrome bus 32 is 18 bits wide (it carries the true and complement of each of the 9 syndrome bits). The inputs to the first stage S1 of each syndrome generator 30S1- 30S9 are subsets of the 128 data bits. Each syndrome generator receives a unique set of data bits, in accordance with the error correction code requirements. In other words, these XOR inputs are wired to calculate the parity of selected subsets of the 128-bit data word according to a parity check matrix defining the error correction code used.

Fig. 1.



As per claim 9, Takemae substantially teaches to check for errors in a memory using parity checking techniques and to correct the detected errors using redundant memory cells. Takemae teaches a semiconductor memory device (col. 1, line 65) with a parity portion and a redundant portion (col. 1, lines 66-68). Takemae teaches an error correcting circuit (col. 2, lines 14-15) to perform error correction. Takemae also teaches to combine the redundant correcting and parity checking process as stated in the present application.

Takemae does not explicitly teach the error correction circuit to use a Hamming code for the correction process as stated in the present application.

However, Fifield, in an analogous art, substantially teaches (abstract) a DRAM which includes an on-chip ECC system. Particularly, Fifield teaches (col. 6, lines 4-23) the error correction circuit to use Hamming code. Fifield also teaches the code length to be less than 72 (col. 2, lines 10-15). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a Hamming code for the correction process in the error correction circuit within the method and apparatus of Takemae. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by utilizing a Hamming code within the error correction circuitry would have improved the error detection and correction capability.

As per claim 10, Takemae substantially teaches, in view of above rejections, (col. 1, lines 17-22) when a defective memory cell is selected to be read, the redundant memory cell is actually read in place of the defective memory cell, so that the correct data can be read.

As per claim 11, Fifield substantially teaches, in view of above rejections, (col. 6, lines 2-23) a Hamming code used in the error correcting circuit which is able detect a double error or

correct a single error. The Examiner would like to point out that Hamming codes are known to have such standardized properties and in fact all error-correcting codes are limited in correcting detected errors. Furthermore, if the code word is found to have more errors than that are correctable, usually it has to be replaced with a redundant code word.

As per claims 12-15, Fifield substantially teaches, in view of above rejections, (Figure 1) syndrome generator 30S1, each generator (or "syndrome tree") is made up of three stage exclusive-OR (XOR) logic trees. The first stage 1S of the logic tree is made up of a first set of four-input XOR gates; the second stage 2S is made up of approximately four four-input XOR gates; and the final stage 3S is a single four-input XOR gate. Note that the syndrome generators 30S1-30S9 have different numbers of inputs (specifically 51, 59, 59, 59, 55, 59, 60, 47, and 56 respectively) to optimize the interconnect wiring layout. The three stages of XOR of one syndrome generator provide the parity of a subset of the one hundred and twenty eight data bits. This generated parity bit is then compared to a corresponding one of the stored check bits for that error correction word. The comparison operation, which is the XOR of a specific subset of PDL lines 15 and their corresponding stored check bits is executed by 1S, 2S and 3S. For the purposes of illustration, assume the arrowhead going into bus 32 is the result of this XOR operation. This XOR result is referred to as a syndrome bit, which is coupled to a respective line of a syndrome bus 32. The syndrome bus 32 is 18 bits wide (it carries the true and complement of each of the 9 syndrome bits). The inputs to the first stage S1 of each syndrome generator 30S1- 30S9 are subsets of the 128 data bits. Each syndrome generator receives a unique set of data bits, in accordance with the error correction code requirements. In other words, these XOR

inputs are wired to calculate the parity of selected subsets of the 128-bit data word according to a parity check matrix defining the error correction code used.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). Applicants are advised to review USPN 6697992, cited in previous office action, as it is particularly pertinent to Applicants' disclosure.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
July 17, 2006

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100